IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Harari		
Title:	Flash EEPROM System with Defective Block Substitution		
Application No.:	09/143,233	Filing Date:	August 28, 1998
Examiner:	Hien N. Nguyen	Group Art Unit:	2824
Docket No.:	SNDK.006UST	Conf. No.:	3263

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APPELLANT'S BRIEF UNDER 37 C.F.R. 41.37

ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

This is in response to the Notice of Non-Compliant Appeal Brief in this application on that was mailed on April 14, 2009. Section III, Status of the Claims, and Section IV, Summary of the Claimed Subject Matter, have been revised. Section II, Related Appeals and Interferences, has also been updated.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is SanDisk Corporation, a corporation of the state of Delaware, the assignee of all right, title and interest in the present patent application from the inventor, Eliyahou Harari.

II. RELATED APPEALS AND INTERFERENCES

Several applications that share disclosure with the present application, all similarly claiming priority from, and limited to the matter disclosed in, US patent application number 07/337,566, have been involved in an appeal, interference, or judicial proceeding. Although they may not have a direct bearing on the present appeal, the following list is provided here through an abundance of caution:

US patent application number 09/103,056 has been involved in Patent Interference No. 104,760. The decision from this Interference is included in the Related Proceedings Appendix.

US patent application number 09/056,398 is involved in Patent Interference No. 105,642 and in Patent Interference No. 105,645.

US patent application number 09/310,880 has been involved in Patent Interference No. 105,606, and the decision in which is currently under appeal.

US patent application number 09/056,398 has been involved in an Appeal. The decision from this Appeal is included in the Related Proceedings Appendix.

A Notice of Appeal and Appeal brief were filed in US patent application number 10/417,954, but the appeal did not go forward and the examiner reopened prosecution. Consequently, there is no decision and the inclusion of one is *not applicable*.

An appeal is currently pending in US patent application number 10/000,155. Consequently, there is as yet no decision and the inclusion of one is *not applicable*.

A Notice of Appeal and Appeal brief were filed in US patent application number 09/114,504, but the appeal did not go forward and the examiner reopened prosecution. Consequently, there is no decision and the inclusion of one is *not applicable*.

US patent number 5,418,752 has been involved in a U.S. International Trade Commission action, Investigation No. 337-TA-382. The decision from this action is included in the Related Proceedings Appendix.

US patent number 5,602,987 has been involved in litigation, *SanDisk Corporation v. Lexar Media, Inc.*, United States District Court for Northern California, San Francisco Division, Case No. C98-0111 CRB (PJH). This case was settled. Consequently, there is no decision and the inclusion of one is *not applicable*.

US patent number 5,602,987 is involved in pending litigation. The decision from an appeal in this case, *SanDisk Corporation v. Memorex Products, Inc.*, 415 F.3d 1278, 75USPQ 2D1475 (Fed. Cir. 2005), is included in the Related Proceedings Appendix.

US patent number 5,719,808 is involved in pending litigation, *STMicroelctronics, Inc. v. SanDisk Corporation v. STMicroelctronics, Inc.*, United States District Court for the Eastern District of Texas, Sherman Division, Case Action No. 4:05CV45. Consequently, there is as yet no decision and the inclusion of one is *not applicable*.

III. STATUS OF THE CLAIMS

Claims 68-78 are on appeal.

The subject application was filed August 28, 1998, and is a continuation of patent application serial no. 08/771,708, filed December 20, 1996, now patent no. 5,991,517, which is a continuation of patent application serial no. 08/174,768, filed December 29, 1993, now patent no. 5,602,987, which is a continuation of patent application serial no. 07/963,838, filed October 20, 1992, now patent no. 5,297,148, which in turn is a division of patent application serial no. 07/337,566, filed April 13, 1989, abandoned. The original parent application claims 1-62 were cancelled in a Preliminary Amendment filed concurrently with the subject application on July 13, 1998. This Preliminary Amendment also added claims 63-67, which were copies of claims 1, 4, 6, 10, and14 of U.S. patent no. 5,668,763 – Fujioka et al. - granted September 16, 1997.

A first Office Action on the merits (mailed December 31, 1998) rejected the pending claims on a double patenting basis and on prior art. A Response (filed April 28, 1999) resulted in these rejections being withdrawn, and was followed by an Office Action (mailed on September 2, 1999, having a one-month non-extendable response period) requiring the

limitations of the claims be applied to the disclosure of the present application. A Preliminary Amendment (filed September 30, 1999, with a Continued Persecution Application) cancelled claims 63-67 in favor of claims 68-74 that were added at that time.

Claims 68-72 and 74 added in the Amendment of September 30, 1999, were either exact copies or closely based on claim 7, 8, 11, 12, 15, and 18, respectively, of US patent number 5,818,754, of Ogura, issued October 6, 1998. An Office Action (mailed December 20, 1999) rejected claims 68-73 on prior art grounds. An Amendment (filed March 17, 2000, and including a Request for Interference) in response added dependent claims 75-78 and led to an Office Action (mailed October 1, 2001, having a one-month non-extendable response period) requiring material that was incorporated by reference to be amended into the specification. To facilitate the application process, this was complied with in an Amendment of October 31, 2001.

Following the Office Action of October 1, 2001, that had a one-month non-extendable response period, the next Office Action was mailed on March 23, 2005, and rejected the claims 68-78 on new grounds under 35 U.S.C.112, first paragraph, as failing to comply with the written description requirement due to the "said second group of memory cells being provided for storing attribute data of said first group of memory cells" and "said attribute data includes a number of rewriting of said first group of memory cells" elements of the claims. A Response (mailed September 19, 2005) argued that the 35 U.S.C. 112, first paragraph, rejection was not well founded and that the written description requirement was met, and further complied with the requirements of U.S.C. 44.202(a)(1)-(6). The subsequent, and most recent, Office Action (mailed on June 7, 2006) again rejected claims 68-78 under 35 U.S.C.112, first paragraph, and made the rejection final.

Claims 68-78 stand rejected under 35 U.S.C. §112, first paragraph, as the Applicants allegedly failed to comply with the written description requirement with respect to the elements of "... storing attribute data ..." and "... a number of rewriting ...".

Consequently, claims 68-78 are on appeal on this basis.

IV. STATUS OF AMENDMENTS

On November 2, 2006, a Notice of Appeal from the Examiner's decision rejecting claims 68-78 was filed. No Amendments have been filed since the June 7, 2006, mailing date of the Office Action from which this Appeal is being taken.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

As background, this section gives a summary of the present invention. Since the claims stand rejected under the written description requirement of 35 U.S.C. §112, first paragraph, some of this material is presented in more detail below in section VII in order to demonstrate that the specification of the subject application meets the written description requirement.

The claimed subject matter is a memory having multiple memory cells arranged along word lines and bit lines. The memory cells are divided into first and second groups, the first group for storing data and the second group for storing information, or attribution data, about the first group: for example, the second group of memory cells may record that number of times that the first group of memory cells has been rewritten.

The pending independent claims are claims 68, 71, and 74.

Claim 68

In claim 68, the memory is presented as:

> 68. A memory comprising:
> a plurality of word lines;
> a plurality of bit lines; and
> a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;
> wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.

In the application, the basic structure of the memory system is discussed in the "EEprom System" section, which begins at the top of page 6. Some of detail on the structure of the memory chips, such as shown in Figures 1 and 2 of the present application, is discussed in more detail in US patent application serial number 204,175, now patent number 5,095,344 ("'344"),

which is incorporated by reference at numerous places in the present application: Figures 15a and 15b of `344 show a memory with each cell corresponding to a selected one of the rows (word lines) and a selected one of the columns (bit lines). The structure is discussed more in section VIII of the `344 patent beginning at column 32, line 57.

The division of the memory cells into a first and second group is shown in Figure 5 of the present application, described beginning at page 16, line 23, of the present application. As described there, a sector of memory cells is divided into a portion 403 and a portion 405, where the portion 403 is for the storage of data. The second portion of memory cells in a sector, 405, includes error correction code (413), defect information (409), and header information (411), all of which are information on the properties of the data stored in the data portion (403) of the sector 401.

This division of memory cells into a first group, which stores data, and a second group, which stores information about the first group, is also disclosed in the `344 patent for the specific case of the number of times that a block of cells has been erased and rewritten. As described there between line 64 of column 28 and line 8 of column 29, the quantity "S" is the number of program/erase cycles to which a block of cells has undergone. The storage of this "S" within the block itself is described at column 29, lines 3-7: "The value of S at any one time can be stored … in each block. Than way each block carries its own endurance history."

Claim 71

Claim 71 differs from 68 in that it is for "a plurality of cell blocks" and that is specifies the size of the "first group of memory cells" rather than specifying that the "attribute data" includes the "number of rewriting". (Consequently, note that ground of rejection based on the "number of rewriting" does not apply to claim 71.) Claim 71 is:

> 71. A memory including a plurality of memory cell blocks, each of said plurality of memory cell blocks comprising:
> a plurality of word lines;
> a plurality of bit lines; and
> a plurality of memory cells, each of said plurality of memory cells being connected between one of said word lines and one of said bit lines;
> wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, wherein said first group of memory cells are provided for storing data and said second group of memory cells are provided for storing

attribute data of said first group of memory cells, and wherein said first group of memory cells are memory cells storing 512 bytes.

In the application, the basic structure of the memory system is discussed in the "EEprom System" section, which begins at the top of page 6. Some of detail on the structure of the memory chips, such as shown in Figures 1 and 2 of the present application, is discussed in more detail in US patent application serial number 204,175, now patent number 5,095,344 ("`344"), which is incorporated by reference at numerous places in the present application: Figures 15a and 15b of `344 show a memory with each cell corresponding to a selected one of the rows (word lines) and a selected one of the columns (bit lines). The structure is discussed more in section VIII of the `344 patent beginning at column 32, line 57.

The division of the memory cells into a first and second group is shown in Figure 5 of the present application, described beginning at page 16, line 23, of the present application. As described there, a sector of memory cells is divided into a portion 403 and a portion 405, where the portion 403 is for the storage of data. The second portion of memory cells in a sector, 405, includes error correction code (413), defect information (409), and header information (411), all of which are information on the properties of the data stored in the data portion (403) of the sector 401. As noted at line 20 on page 15, a sector size is typically 512 bytes.

Claim 74

Claim 74 differs from 68 in that it is specifies "a plurality of cell blocks":

74. A memory comprising:
a plurality of memory cell blocks further comprising;
a plurality of word lines;
a plurality of bit lines; and
a plurality of memory cells, wherein each of said plurality of memory cells corresponds to a selected one of said word lines and a selected one of said bit lines; and wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells provided for storing data and said second group of memory cells provided for storing attribute data of said first group of memory cells, and wherein said attribute data includes a rewriting number of said first group of memory cells.

In the application, the basic structure of the memory system is discussed in the "EEprom System" section, which begins at the top of page 6. Some of detail on the structure of the memory chips, such as shown in Figures 1 and 2 of the present application, is discussed in more detail in US patent application serial number 204,175, now patent number 5,095,344 ("`344"),

which is incorporated by reference at numerous places in the present application: Figures 15a and 15b of `344 show a memory with each cell corresponding to a selected one of the rows (word lines) and a selected one of the columns (bit lines). The structure is discussed more in section VIII of the `344 patent beginning at column 32, line 57.

The division of the memory cells into a first and second group is shown in Figure 5 of the present application, described beginning at page 16, line 23, of the present application. As described there, a sector of memory cells is divided into a portion 403 and a portion 405, where the portion 403 is for the storage of data. The second portion of memory cells in a sector, 405, includes error correction code (413), defect information (409), and header information (411), all of which are information on the properties of the data stored in the data portion (403) of the sector 401.

This division of memory cells into a first group, which stores data, and a second group, which stores information about the first group, is also disclosed in the `344 patent for the specific case of the number of times that a block of cells has been erased and rewritten. As described there between line 64 of column 28 and line 8 of column 29, the quantity "S" is the number of program/erase cycles to which a block of cells has undergone. The storage of this "S" within the block itself is described at column 29, lines 3-7: "The value of S at any one time can be stored … in each block. Than way each block carries its own endurance history."

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Board is asked to review the correctness of the rejections under 35 U.S.C. §112, first paragraph. Specifically, claims 68-78 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement with respect to both the "storing attribute data" and the "number of rewriting" elements of the claims. The Office Action alleges that the specification provides no written description with respect to these two points:

a) "there is no support for the recitation of 'said second group of memory cells being provided for ***storing attribute data*** of said first group of memory cells'".

b) "there is no support for 'said attribute data includes a ***number of rewriting*** of said first group of memory cells'". [emphases original in Office Action for both quotes]

These are the bases for rejecting all of the claims and are the sole issues in this appeal, although it is noted that second of these is not applicable to independent claim 71 and its dependents as they do not include the "number of rewriting" limitation.

All of the claims stand rejected under the first of these grounds and can be taken to form a single group; the second ground of rejection is correctly applicable to claims 68-70 and 74-78, which and can be taken to form a single group. In both cases, independent claim 68 is suitable for deciding whether the group of claims is patentable.

VII. ARGUMENT

The most recent Office Action, from which this Appeal originates, rejects all of the pending claims under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement for two reasons, as described in the preceding section. All of the claims are rejected on the first of these grounds, and, although the Office Action rejects all of the claims on the second of these grounds, the limitation at the base of the second ground is only present in claims 68-70 and 74-78. In both cases, all of the claims are argued together and, when reference to a specific claim is required, claim 68 is believed suitable for this purpose. Each of the different points noted in the last section will be treated under the corresponding sub-heading below. In each case, it is believed that the needed written description requirement is met.

It should be noted that even though the Office Action treats these two grounds of rejection as distinct, and that they are argued separately below, that they are, in fact, related: as the "number of rewriting" is an example of "attribute data", support for the first of these (discussed under point b) below) consequently is support for the second of these (discussed under a) below).

a) "said second group of memory cells being provided for storing attribute data of said first group of memory cells"

The Office Action states:

> a) there is no support for the recitation of "said second group of memory cells being provided for ***storing attribute data*** of said first group of memory cells". The full specification **did not** disclose what is considered as an attribute data or what is a function of storing between two different groups of memory cells. ... There is no discussion, explicitly or impliedly, that this portion is used for storing attribute data.

> Furthermore, there is no suggestion that this area may or can be used as an attribute data storage. Accordingly, there is no description in the specification to support the recitation of "storing attribute data" or "attribute data". [emphasis in Office Action]

It is believed that not only does the present application provide written description of the cited limitation, but that the Office Action is also reading limitations into the claim, improperly interpreting the claim, or both.

In the present application, Figure 5 shows a memory architecture where the memory cells in a sector 401 are organized as a data portion 403, where user data is stored, and a shadow portion 405, in which information on the properties the sector and its data is stored. This is described in the present application at page 16, lines 24-35:

> As described before, the Flash EEprom memory is organized into sectors where the cells in each sector are erasable together. The memory architecture has a typical sector 401 organized into a data portion 403 and a spare (or shadow) portion 405. The data portion 403 is memory space available to the user. The spare portion 405 is further organized into an alternative defects data area 407, a defect map area 409, a header area 411 and an ECC and others area 413. These areas contain information that could be used by the controller to handle the defects and other overhead information such as headers and ECC.

Thus, the memory cells are divided into a first group of memory cells for storing data, namely the data portion 403, and a second group of memory cells, namely the shadow portion 405. This second group of memory cells 405 includes error correction code (413), defect information (409), and header information (411), all of which are data on the properties, or attributes, of the data stored in the first group of memory cells 403. Consequently, the present application provides written description of that the "plurality of memory cells are divided into a first group of memory cells [403] and a second group of memory cells [405], said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data [e.g., error correction code, defect information, header information] of said first group of memory cells".

Consequently, it is submitted that the specification clearly describes having one group (the "second group") of memory cells being provided for storing data on the properties of another group (the "first group") of data storing memory cells; hence, the "second group" of memory cells stores attribute data on the "first group" of memory cells. Thus, this rejection does not appear proper under the first paragraph of 35 U.S.C. §112 since, as described above, the specification is believed to supply more than an adequate written description of these claims.

The Office Action is correct in so far as that the specification does contain the *exact phrase* of "attribute data"; however, this is a much more stringent requirement than is needed to satisfy the written description requirement of 35 U.S.C. §112, first paragraph, and is an improper basis for a rejection. As discussed in detail in the M.P.E.P. at §2111, and specifically in §2111.01, "The words of a claim must be given their 'plain meaning' unless they are defined in the specification". There is nothing in specification of the present application that defines "attribute data" to have anything other than its plain meaning, namely information on the properties of something (namely, the first group of data storing cells), which the specification clearly describes the spare (or shadow) portion of memory cells as being.

In its "Response to Amendment" section, the Office Action states (beginning at line 8 of page 5):

> Even though the definition of "attribute" has a broad definition in an English dictionary, the meaning in the field of "nonvolatile memory" does have a specific definition and have a particular function for a specific feature in separate situation in order for a person of ordinary skill in the art to understand and make use of it. Thus, unless the term "attribute" is defined. It is merely a term with no specific function associated therewith. Another word, it has to be defined clearly and specifically and it has to be used consistently in the whole application in order to be consider for patentability. [sic, emphasis original in Office Action]

These remarks seem to turn the requirements of M.P.E.P. §2111 on its head by apparently taking it to require a "specific definition" (such as, say, "an attribute is hereby defined to be a property") of what is a clearly an understandable phrase whose plain meaning is clearly met.

The specification of the present application describes that the one group of memory cells are used to store information on properties or qualities (such as error correction code, defect information, header information) of another group of memory cells that store user data. This clearly describes the storing of data on the attributes of the memory cells storing user data. Instead, the Office Action has apparently further required, however, a "specific definition". This point is considered in the third paragraph of section 2163.02 of the M.P.E.P.. This states (where the emphasis has been added) that:

> The subject matter of the claim **need not be described literally (i.e., using the same terms or *in haec verba*)** in order for the disclosure to satisfy the description requirement.

Thus, not only is it respectfully submitted that the written description requirement is met, but that the Examiner is further asking for a requirement that is clearly contrary to this explicit statement.

The "Burden on the Examiner with Regard to the Written Description Requirement" is the subject of section 2163.04 of the M.P.E.P.. This states (where the emphasis has been added) that:

> ... A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. ... The examiner, therefore, must have a reasonable basis to challenge the adequacy of the written description. *The examiner has the initial burden of presenting* ***by a preponderance of evidence*** *why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims.*

It is respectfully submitted that not only has the Examiner failed to present "a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims", but has rejected the pending claims on a requirement that is contrary to the explicit criteria of the M.P.E.P..

Considering the Response to Arguments portion of the Office Action, it should again be noted that claim 68 of the present application is copied from US patent number 5,818,754. Based on the comments in its "Response to Amendment" (beginning at page 5, line 8 of the Office Action), the Office Action seems to be requiring that present application provide not just support for the claims as written, but for how a specific term is used in of US patent number 5,818,754. This is improper. The Office Action appears to be reading limitations of a specific embodiment of this patent into the claim and then requiring the present application to support this particular embodiment. The correct question is whether the present specification is enabling for the claim ***as written***.

Besides being improper, as an aside it should also be noted that this analysis of the Office Action is incorrect. Even if "attribute data" were a term of art (or even if any "specific definition" of this term were imported from US patent number 5,818,754), US patent number 5,818,754 describes "attribute data" as follows at column 2, lines 15-19:

> The attribute memory 22 is necessary for a computer system, not illustrated, using the IC memory card to store various information (hereinafter, attribute data) for normally using the IC memory card.

That is, "attribute data" is just "information .... for normally using the ... memory card", which the various information stored in the "spare (or shadow) portion 405" of the present application

clearly is. In any case, it should be noted that the one example of "attribute data" given in US patent number 5,818,754, namely the number of times which the data cells have been rewritten, is itself disclosed in the present application, as discussed under heading b) that follows below.

Consequently, for any of the reasons above, this rejection also does not appear proper under the first paragraph of 35 U.S.C. §112. As described above, the specification is believed to more than satisfy the written description require for "said second group of memory cells being provided for storing attribute data of said first group of memory cells".

b) "said attribute data includes a number of rewriting of said first group of memory cells"

Concerning this limitation, the Office Action states:

> b) there is no support for "said attribute data includes a ***number of rewriting*** of said first group of memory cells". As admitted by the applicant Amendment (also by the disclosure and figure 9), the number (S) is the number of full erase cycles experienced by a block in a sequence of erase algorithm. This number (S) can be used as a preset number to avoid excessive erasing. Thus, **this number (S) is a number of full erase cycles and is not related to** *"a number of rewriting of a first group of memory cells"* and such description cannot be relied upon for support of this claim recitation. [emphases in Office Action]

It is believed that not only does the present application provide written description of the cited limitation, but that the Office Action is again also reading limitations into the claim, improperly interpreting the claim, or both; further, this statement of the Office Action contains a number of mistakes or inconsistencies.

The storage of the number of times that a group of memory cells has been rewritten is disclosed in the present application by virtue of its disclosure in US patent application serial number 204,175, now patent number 5,095,344 ("'344"), which is incorporate by reference at numerous places in the present application. Specifically, at column 28, line 64, to column 29, line 7, the '344 patent states:

> The number S of complete erase cyclings experienced by each block is an important information at the system level. If S is known for each block then a block can be replaced automatically with a new redundant block once S reaches $1X10^6$ (or any other set number) of ***program/erase cycles***. S is set at zero initially, and is incremented by one for each complete block erase multiple pulse cycle. *The value of S at any one time can be stored* by using for example twenty bits (2^{20} equals approximately $1X10^6$) *in each block.* That way *each block carries its own endurance history.*

As the added emphasis indicates, the value S indicates the number of number of times that the data cells of the block have been erased and reprogrammed. As the value S itself is also stored in the block, one group of memory cells in the block (where S is stored) store the number of times that another group of memory in the block (the data cells) have been rewritten (the value of S).

(As an aside, it should be noted that the Office Action has not objected to the use of this material incorporated by reference in order to meet the written description requirement: this is not at issue here and the material of `344 patent forms an integral part of the specification by virtue of its incorporation by reference. Rather, the Office Action asserts that this incorporated material does not meet the written description requirement.)

In any case, based on the quote from Office Action at the beginning of this subsection, it appears that the Office Action fully acknowledges that the present application satisfies the written description requirement with respect to the quantity "S", but that the basis of Office Action's rejection is contained in the statement found in the last sentence of this quote: "**this number (S) is a number of full erase cycles and is not related to** *'a number of rewriting of a first group of memory cells' …*", where all the emphases are again original to the Office Action. It is respectfully submitted that this statement of the Office Action is incorrect. The exemplary embodiments of the present invention use EEprom based memory cells. It is basic to the operation of such devices that, prior to being reprogrammed, they are erased. This is described in the present application, for example, in the "Erase of Memory Structures" section that begins on line 6 of page 8. Thus, as stated there at lines 12-15:

> In a Flash EEprom memory, the memory cells must first be erased before information is placed in them. That is, a write (or program) operation is always preceded by an erase operation.

The basic operation of EEprom devices are also discussed in great detail in the "Detailed Description of the Prior Section (column 5, line 31) and elsewhere in the `344 patent (which, among the various places it is incorporated by reference into the present application, is incorporated specifically with respect to "[o]ptimized erase implementations" at page 11, lines 23-29). Further, the quotation in the last paragraph itself states "once ***S*** reaches $1X10^6$ (or any other set number) of ***program/erase cycles***", where the emphasis is again added.

(Additionally, the Office Action is incorrect when it states: "This number (S) can be used as a preset number to avoid excessive erasing." Rather, S not held at a set value, but is incremented at each program/erase cycle and it is the maximum value of S that is set.)

Consequently, it is submitted that the specification clearly describes having one group (the "second group") of memory cells being provided for storing data on the number of times that another group (the "first group") of data storing memory cells has been rewritten; hence, the "second group" of memory cells stores the "number of rewriting" of the "first group" of memory cells. Thus, this rejection does not appear proper under the first paragraph of 35 U.S.C. §112 since, as described above, the specification is believed to supply more than an adequate written description of these claims.

The Office Action is correct in so far as that the specification does contain the *exact phrase* of "number of rewriting"; however, as already discussed in the last subsection, this is a much more stringent requirement than is needed to satisfy the written description requirement of 35 U.S.C. §112, first paragraph, and is an improper basis for a rejection. As discussed in detail in the M.P.E.P. at §2111, and specifically in §2111.01, "The words of a claim must be given their 'plain meaning' unless they are defined in the specification". There is nothing in specification of the present application that defines "number of rewriting" to have anything other than its plain meaning, namely the number of times that a memory cell has been through an erase/program cycle, which the specification clearly describes the parameter "S" as being.

In its "Response to Amendment" section, the Office Action states (beginning 5 lines from the bottom of page 5):

> **b)** Regarding the response of the rejection based on lack of support of limitation ***"rewriting number"*** *in the Remarks on page 6, the applicant continued to stretch* ***"the quantity "S" is the number of*** *"program/erase cycles"* ***and thus corresponds to the "rewrite number" of the first group of memory cells".***
> Again the Examiner found no relation of *"a counter of erase cyclings"* as adequate equivalent support meaning of *"a rewriting number"* in the field of "nonvolatile memory". Further, the word of "rewrite" or "a function of rewriting" can not be found anywhere in the passage below as shown in the Remarks [of previous amendment] on page 6, quoting its support in the parent patent as follow:
>
> > [quote from column 28, line 64, to column 29, line 7, the `344 patent states given above, deleted]
>
> Thus, the rejection of the claims as lacking support for the recitation of "rewriting number" is deemed proper and has not been persuasively rebutted. [sic, all emphases original in Office Action]

These remarks again seem to turn the requirements of M.P.E.P. §2111 on its head by apparently taking it to require the use of the exact word "rewrite", where the specification used of what is a clearly an understandable phrase, number of "program/erase cycles", whose plain meaning is clearly the number of times that a cell has been rewritten. In fact, *it is basic to the operation of EEprom devices that the rewriting of the data content of a memory cell requires the cell to be erased prior to being reprogrammed.* Reference is again made to the third paragraph of section 2163.02 of the M.P.E.P. (where the emphasis has been added):

> The subject matter of the claim **need not be described literally (i.e., using the same terms or *in haec verba*)** in order for the disclosure to satisfy the description requirement.

Thus, not only is it respectfully submitted that the written description requirement is met, but that the Examiner is again further asking for a requirement that is clearly contrary to this explicit statement.

The "Burden on the Examiner with Regard to the Written Description Requirement" is the subject of section 2163.04 of the M.P.E.P.. This states (where the emphasis has been added) that:

> ... A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. ... The examiner, therefore, must have a reasonable basis to challenge the adequacy of the written description. *The examiner has the initial burden of presenting* ***by a preponderance of evidence*** *why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims.*

It is respectfully submitted that not only has the Examiner failed to present "a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims", but has rejected the pending claims on a requirement that is contrary to the explicit criteria of the M.P.E.P.. In, it is again that the Office Action's statement that "**this number (S) is a number of full erase cycles and is not related to** *'a number of rewriting ...'* [emphases in Office Action] is not only incorrect, but contrary to the basic operation of EEprom based memory cells and that "a person skilled in the art" would understand this to be the case.

Consequently, for any of the reasons above, this rejection also does not appear proper under the first paragraph of 35 U.S.C. §112. As described above, the specification is believed to more than satisfy the written description require for "said second group of memory cells being

provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.

VIII. CONCLUSION

It is Applicants' position, as indicated above, that the assertions of the Office Action are incorrect. In each of the cases described above, it is believed that disclosure provided by the subject application meets the written description requirement. Accordingly, the rejection of the application should be reversed and the present patent application passed to issue.

Respectfully submitted,

_____	8/12/09
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Appendix A

CLAIMS PENDING IN APPLICATION SERIAL NO. 09/143,233

Claims 1-67 are cancelled.

68. A memory comprising:

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;

wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.

69. A memory as claimed in claim 68, wherein said first group of memory cells and said second group of memory cells are accessible by a common sector address.

70. A memory as claimed in claim 68, further comprising an erasing circuit to erase data stored in at least one or more of said plurality of memory cells in response to an erasing signal.

71. A memory including a plurality of memory cell blocks, each of said plurality of memory cell blocks comprising:

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells, each of said plurality of memory cells being connected between one of said word lines and one of said bit lines;

wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, wherein said first group of memory cells are provided for storing data and said second group of memory cells are provided for storing attribute data of said first group of memory cells, and wherein said first group of memory cells are memory cells storing 512 bytes.

72. The memory as claimed in claim 71, further comprising an erasing circuit to erase contents of all of said plurality of memory cells in response to an erasing signal.

73. The memory as claimed in claim 71, wherein said first group of memory cells and said second group of memory cells are accessed by a common sector address.

74. A memory comprising:

a plurality of memory cell blocks further comprising;

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells, wherein each of said plurality of memory cells corresponds to a selected one of said word lines and a selected one of said bit lines; and wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells provided for storing data and said second group of memory cells provided for storing attribute data of said first group of memory cells, and wherein said attribute data includes a rewriting number of said first group of memory cells.

75. The memory as claimed in claim 69, further comprising an erasing circuit to erase contents of all of said memory cells accessible by a common sector address in response to an erasing signal.

76. The memory as claimed in claim 73, further comprising an erasing circuit to erase contents of all of said memory cells accessible by a common sector address in response to an erasing signal.

77. The memory as claimed in claim 74, wherein said first group of memory cells and said second group of memory cells are accessed by a common sector address.

78. The memory as claimed in claim 77, further comprising an erasing circuit to erase contents of all of said memory cells accessible by a common sector address in response to an erasing signal.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

DECISION ON PRELIMINARY MOTIONS
PATENT INTERFERENCE NO. 104,760

DECISION ON YAMAGAMI SECOND REQUEST FOR RECONSIDERATION AND FINAL JUDGMENT, PATENT INTERFERENCE NO. 104,760

DECISION ON APPEAL, APPEAL NO. 2001-1272
U.S. INTERNATIONAL TRADE COMMISSION, INVESTIGATION NO. 337-TA-382

DECISION ON APPEAL, *SANDISK CORPORATION V. MEMOREX PRODUCTS, INC.*, 415 F.3D 1278, 75USPQ 2D1475 (FED. CIR. 2005)